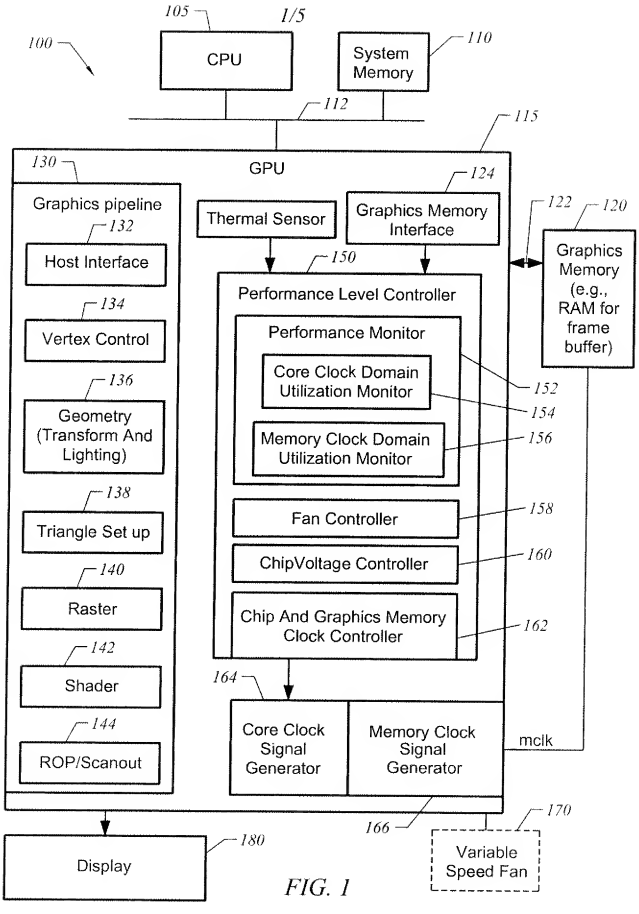
1/5
100
105
CPU
System Memory
110
112
115
130
GPU
Graphics pipeline
132
Host Interface
134
Vertex Control
136
Geometry (Transform And Lighting)
138
Triangle Set up
140
Raster
142
Shader
144
ROP/Scanout
Thermal Sensor
124
Graphics Memory Interface
122
120
Graphics Memory (e.g., RAM for frame buffer)
150
Performance Level Controller
Performance Monitor
Core Clock Domain Utilization Monitor
152
154
Memory Clock Domain Utilization Monitor
156
Fan Controller
158
ChipVoltage Controller
160
Chip And Graphics Memory Clock Controller
162
164
Core Clock Signal Generator
Memory Clock Signal Generator
mclk
166
170
Variable Speed Fan
180
Display

FIG. 1

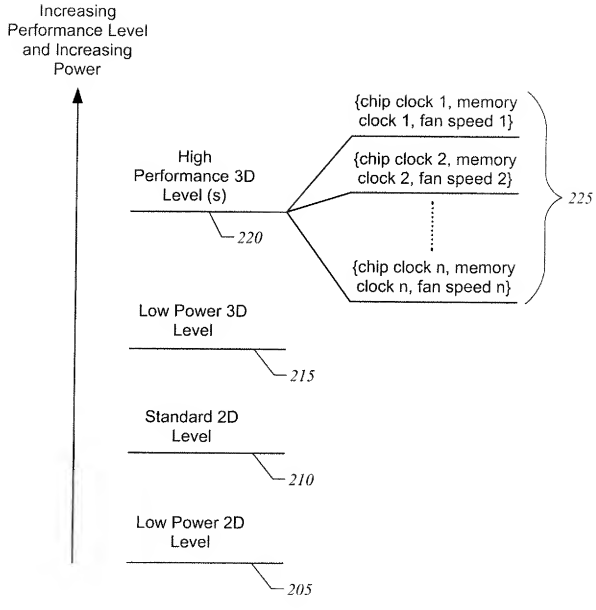
Increasing Performance Level and Increasing Power
High Performance 3D Level (s)
220
{chip clock 1, memory clock 1, fan speed 1}
{chip clock 2, memory clock 2, fan speed 2}
{chip clock n, memory clock n, fan speed n}
225
Low Power 3D Level
215
Standard 2D Level
210
Low Power 2D Level
205

FIG. 2

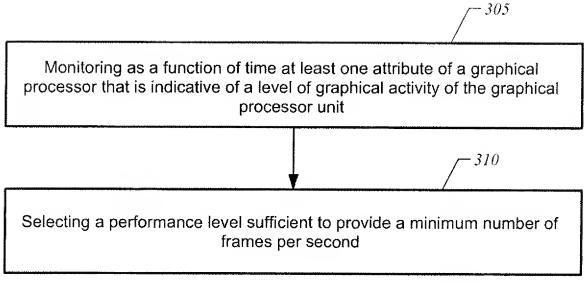
305
Monitoring as a function of time at least one attribute of a graphical processor that is indicative of a level of graphical activity of the graphical processor unit
310
Selecting a performance level sufficient to provide a minimum number of frames per second

FIG. 3

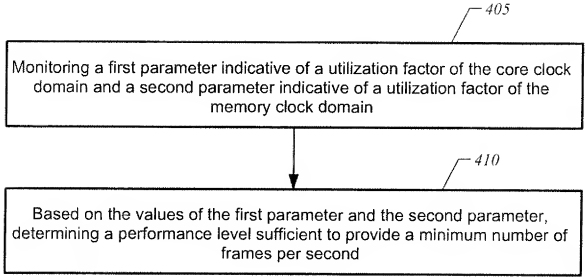
405
Monitoring a first parameter indicative of a utilization factor of the core clock domain and a second parameter indicative of a utilization factor of the memory clock domain
410
Based on the values of the first parameter and the second parameter, determining a performance level sufficient to provide a minimum number of frames per second

FIG. 4

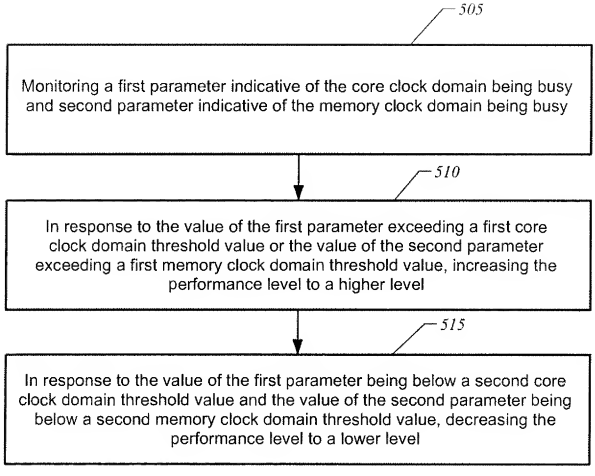
505
Monitoring a first parameter indicative of the core clock domain being busy and second parameter indicative of the memory clock domain being busy
510
In response to the value of the first parameter exceeding a first core clock domain threshold value or the value of the second parameter exceeding a first memory clock domain threshold value, increasing the performance level to a higher level
515
In response to the value of the first parameter being below a second core clock domain threshold value and the value of the second parameter being below a second memory clock domain threshold value, decreasing the performance level to a lower level

FIG. 5